Research Article **ISSN: 2395 – 5597**

International Journal of Engineering and Robot Technology

Journal home page: www.ijerobot.com

https://doi.org/10.36673/IJEROBOT.2025.v12.i01.A01

LOW POWER SCALABLE SORTING NETWORK USING GDI-BASED MAGNITUDE COMPARATOR AND WEIGHTED BITSTREAM CONVERSION

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ABSTRACT

In this paper, a low power, scalable sorting network is designed by integrating a Gate Diffusion Input (GDI) - based magnitude comparator and an enhanced weighted bitstream converter. The bit-stream converter is extended to support 4-bit, 8-bit, 16-bit and 32-bit inputs, generating accurate weighted bit-streams in just n clock cycles instead of 2n. The magnitude comparator from the sorting block is redesigned using GDI logic to significantly reduce power consumption compared to conventional CMOS logic, Power and delay metrics are evaluated under identical conditions.

KEYWORDS

Magnitude comparator, Gate diffusion input logic, Sorting block, Bitstream converter and Power optimization.

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INTRODUCTION

In recent trends of VLSI system design, low power consumption, low latency and high scalability have become ever more critical with the increasing need for portable, energy-efficient and high-performance computing platforms. Embedded systems, real-time signal processing systems and edge computing systems must stay within hard power and area constraints while still demanding rapid and dependable processing capabilities. Among numerous operations within digital systems, sorting is a common and computation-intensive operation used in image and video processing, data mining, networking and database systems, among others. Nonetheless, achieving efficient hardware-based

sorting modules conforming to the requirements of power, performance and area continues to be a major challenge.

Optimization at the comparator level a basic component in sorting networks is essential to address these requirements. The magnitude comparator is one of the most important components that determine the relative ordering between the inputs in a sorting system. Classic CMOS-based comparator designs, while being accurate, are far from ideal in power, transistor size, and switching activity. Therefore, the Gate Diffusion Input (GDI) approach is followed in this project for designing the magnitude comparator. GDI logic supports the creation of small, low-power logic gates by minimizing the transistors needed for elementary operations, reducing the dynamic and leakage power. The GDI-based magnitude comparator proposed in this paper extensively reduces the power and area overhead over traditional logic, but it is very applicable to scalable VLSI sorting architectures.

Although improving the comparator is crucial, substituting legacy compare-and-swap (CAS) sorting networks with a more effective design is just as critical for minimizing latency and power. For this project, the Lock-and-Swap (LAS) sorting network[1] design is used, following recent publications that present weighted stochastic bitstreams. In contrast to traditional Stochastic Computing[2], which is plagued by long bitstream lengths and exponential latency (2^n cycles for n-bit data), weighted bitstreams maintain the weight of binary values and support linear scaling (n cycles), significantly decreasing the number of processing cycles. The LAS block serves as an advanced CAS unit by fixing the comparison result as soon as the first different bit between two weighted bitstreams is reached. This process not only reduces redundant computation but also guarantees deterministic response appropriate for high-speed digital circuits.

One of the key contributions of this work is the extension and integration of weighted bitstream converters to data widths of 4-bit, 8-bit, 16-bit and 32-bit inputs. Such converters convert binary inputs to linearly scaled weighted bitstreams that preserve the binary significance of the data, which allows for accurate yet efficient bitstream-based computation. The designed approach obviates the need for typical stochastic number generators and long counters, which would otherwise be resource-hungry.

In this work, the GDI-based magnitude comparator is integrated into every LAS unit in the sorting network, offering energy-efficient comparison operations. The LAS sorting network constructed from these comparators performs parallel processing and makes early decisions, thus lowering latency and energy usage. Expanding this architecture to support different bit-widths, the design proves its scalability and flexibility for practical applications in VLSI.

This work counters the major limitations of conventional sorting networks i.e., high area, power, and latency by harnessing the combined power of GDI logic, weighted bitstream conversion and LAS-based sorting structure. The system proposed here is a low-power, high-speed and scalable sorting in VLSI applications with particular emphasis on situations where hardware resources are limited and performance is important.

LITERATURE REVIEW

Sorting networks play a crucial role in high-speed applications like image processing, signal filtering, and switching systems because they can process data consistently and at the same time. However, traditional compare-and-swap (CAS) sorting networks, such as Batcher and Bitonic networks, often require a lot of hardware. They also tend to use a large amount of area and power as data resolution increases. Recent research has focused on developing designs that use less power and take up less space through logic optimization techniques. One promising method is the Gate Diffusion Input (GDI) logic technique. This method allows for the creation of compact and energy-efficient logic gates with fewer transistors than typical CMOS designs. Incorporating GDI-based magnitude comparators in sorting networks can lower switching activities and leakage power, leading to better performance in VLSI systems.

Additionally, weighted bitstream conversion has gained popularity in stochastic and unary-based processing systems. This technique transforms

binary inputs into bitstreams that represent their values as a fraction of 1s. It simplifies arithmetic operations in hardware by encoding data in time or probability domains, making it suitable for power-sensitive applications. Using GDI-based comparators in bitstream sorting architectures enhances median filtering and data ranking. This approach ensures efficiency, scalability and low energy use. This mixed design strategy holds great promise for future systems, particularly in low-power image processing and embedded computing.

GDI-BASED MAGNITUDE COMPARATOR

A magnitude comparator is a digital circuit designed to compare two binary numbers and figure out their sizes. It shows the result of the comparison, indicating whether one number is greater than, less than, or equal to the other. The process starts with the most significant bit (MSB) and moves down to the least significant bit (LSB), comparing the two binary inputs bit by bit. If it finds a difference at any bit position, it uses that bit to determine the result and ignores the rest. You'll often find magnitude comparators in digital systems where comparing values is essential, like in sorting algorithms, decision-making circuits, and arithmetic operations.

The low-power digital logic design technique called Gate Diffusion Input (GDI) changes the game for creating complex logic functions. It uses significantly fewer transistors than traditional CMOS logic. This GDI style reduces short-circuit power and improves switching speed. It is an excellent choice for low-power VLSI designs, particularly in embedded and portable systems.

GDI logic uses a configuration where inputs are applied to the source, gate and drain of transistors, enabling designs that are simpler and more compact with fewer transistors than conventional logic styles.GDI proves very beneficial in magnitude comparator implementations, as it reduces transistor counts, power consumption, switching activities, and layout area.

The GDI-based magnitude comparator achieves the same functionality but with a more simplified structure. This leads to a small and power-efficient comparator, which is essential when such comparators need to be reused repeatedly in architectures such as sorting networks. By designing a magnitude comparator using Gate diffusion input logic, the power decreases by 98.59% from conventional CMOS logic.

SORTING NETWORK

A sorting network is a static hardware device consisting of a series of Compare-and-Swap (CAS) blocks that sort a fixed number of inputs. In contrast to software implementations of algorithms, sorting networks are deterministic and permit high parallelism, thus being most suitable for pipelined and real-time systems. Conventional networks, however, are resource-intensive with increasing input size as they depend upon binary comparators and multiplexers. High-performance blocks such as Lock-and-Swap (LAS), units provide further improvement in performance through early decision-making and reduced switching activity.

LOCK AND SWAP SORTING NETWORK

The Lock-and-Swap (LAS) block[1] is, a low-energy replacement for the conventional Compare-and-Swap (CAS) unit of sorting networks. It works on the same fundamental task, sorting two inputs into minimum and maximum but in terms of timing and energy consumption with an improvement. The most important innovation of the LAS block is the locking of the comparison result as soon as the first difference between two input weighted bitstreams is identified. This initial decision-making saves processing the complete bitstream, and hence reduces latency from 2^n to n cycles for n-bit inputs. The LAS block has two primary registers: a Lock register to store the decision of comparison, and a Swap register to decide whether or not the inputs are to be swapped according to the difference detected.

The decision, once locked, is retained by the LAS unit for the rest of the cycles, thereby preventing unnecessary switching, which reduces dynamic power usage. Moreover, the LAS structure is more scalable and more modular and thus it is most suitable for sorting large bit-width data in parallel.

WEIGHTED BITSTREAM CONVERTER

The bitstream converter is an essential element that facilitates the utilization of weighted stochastic bitstreams within digital systems. It transforms regular binary inputs into weighted bitstreams[1], where every bit retains its positional weight. This makes bitstream-based processing capable of projecting real binary magnitude without the need for lengthy stochastic sequences. The converter is made up of shift registers (REGs) and multiplexers (MUXs) that serialize the binary information into a stream, preserving direction and bit order. The reset signal resets the converter to allow for repeated conversions. The same piece of hardware can also be reversed to convert bitstreams back into binary, hence bi-directional. The converter also simplifies hardware by eliminating random number generation and large counters employed in conventional SC.

PROPOSED DESIGN

The proposed architecture is introducing the energy-efficient Gate Diffusion Input (GDI)-based magnitude comparator in a hardware-based sorting module to maximize power, area, and delay parameters. The proposed scheme takes advantage of the small size of GDI logic, which consumes less transistor count compared to the conventional CMOS scheme, allowing high-speed operation with drastically lower power consumption.

In this sorting architecture, the magnitude comparator constitutes the primary decision-making component that conducts element-wise comparisons to ascertain ordering between input values. Replacing traditional comparators with GDI-based comparators minimizes overall switching activity and leakage power, thus making the design appropriate for low-power and high-speed applications, particularly in portable or battery-powered systems.

Scalable Implementation

To demonstrate scalability and adaptability, the proposed sorting unit has been implemented for multiple input sizes.

4-bit Sorting Unit

This simple setup is a proof of concept and assures the fundamental logic. It is suitable for small embedded systems with minimal sorting needs.

8-bit and 16-bit Sorting Units

These implementations expand the logic to support more advanced operations, providing a compromise between resource consumption and sorting accuracy.

32-bit Sorting Unit: Designated for high-speed applications, this model can sort big data values, which is ideal for digital signal processing (DSP), image processing and high-speed communication systems.

IMPLEMENTATION RESULT

The GDI-based magnitude comparator simulation was done using Tanner EDA for different input word lengths-4-bit, 8-bit, 16-bit, and 32-bit. The outcome depicts considerable improvements in both power efficiency and propagation delay over the conventional 4-bit design. The proposed 4-bit design consumes 14μW, which is slightly less than the conventional 15μW, with decreased delay of 2 ns compared to 2.5 ns, making it the performance benchmark.

As bit-width is scaled, power consumption from 19μW (8-bit) to 128 μW (32-bit) increases, corresponding to the increase in power by 1.36× to 8.54× from the 4-bit reference. Likewise, the delay from 4.3 ns to 8.8 ns goes up, which is 2.15× to 4.40× more than the 4-bit design. These findings suggest that although power and delay increase with bit-width, the GDI-based structure shows improved efficiency and reduced overhead than traditional logic due to its scalability and low-power nature, being an efficient and low-power hardware-based sorting unit solution.

Table No.1: Comparison result

S.No	Design	Power (uw)	Power increased from 4 bit	Delay (ns)	Delay increased from 4 bit
1	4-bit Conventional	15	-	2.5	-
2	4-bit	14	1-baseline	2	1-baseline
3	8-bit	19	1.36x	4.3	2.15x
4	16-bit	58	4.16	6	3.00x
5	32-bit	128	8.54	8.8	4.40x

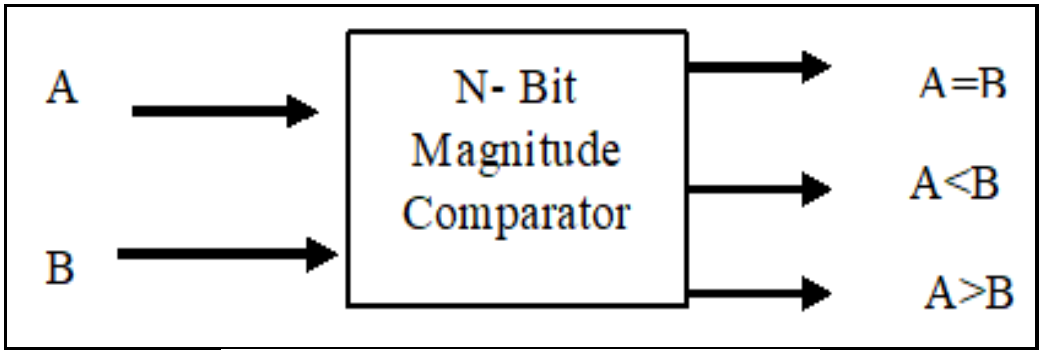

Figure No.1: N-bit Magnitude Comparator

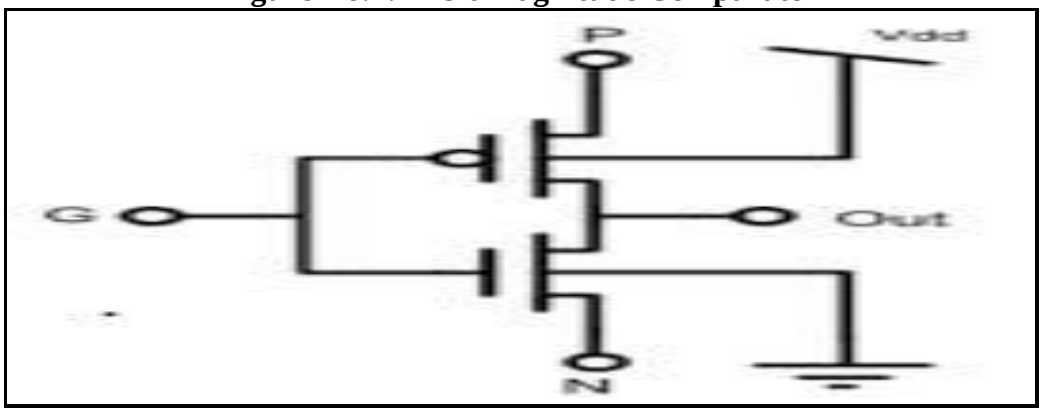

Figure No.2: Basic GDI cell

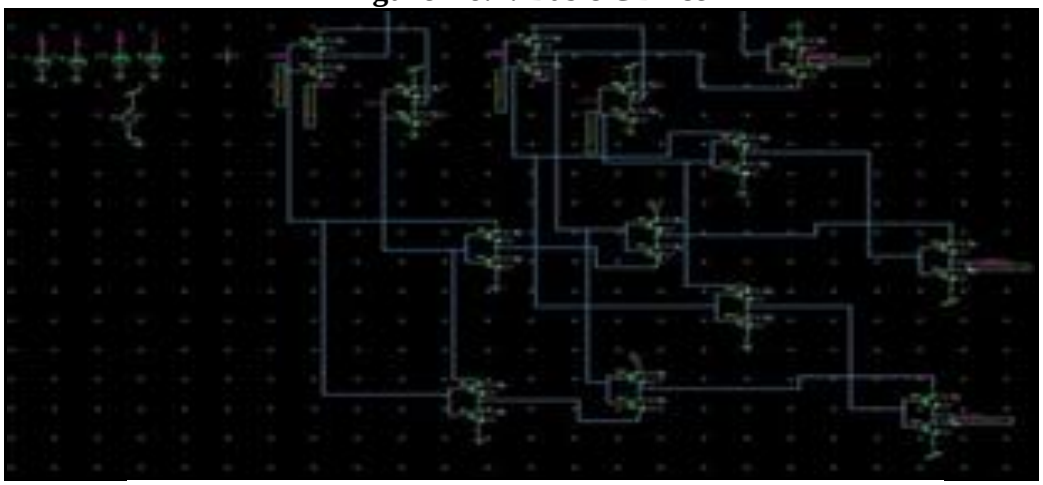

Figure No.3: 2-bit Magnitude Comparator using GDI logic

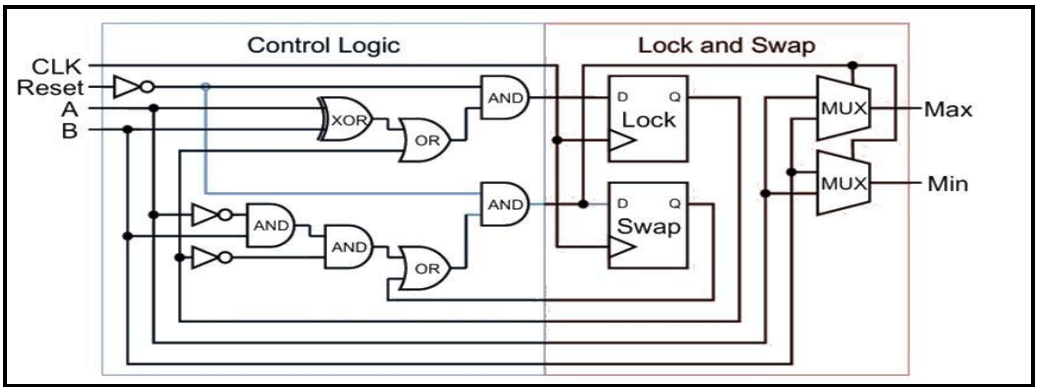

Figure No.4: Lock and Swap sorting network

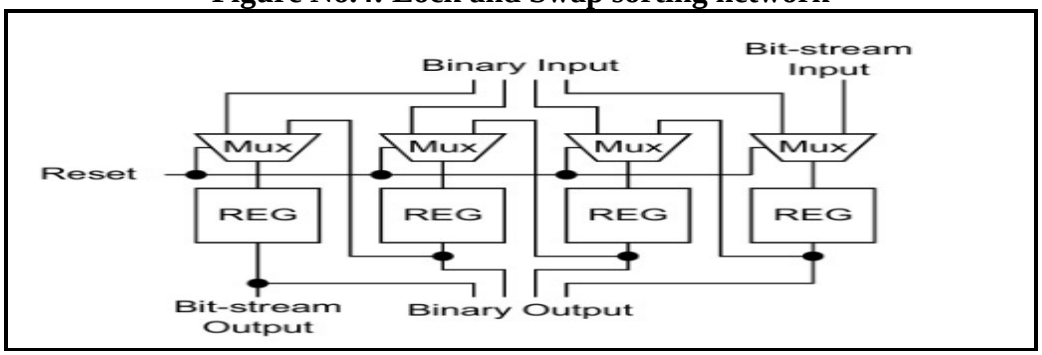

Figure No.5: 4-bit weighted bitstream converter

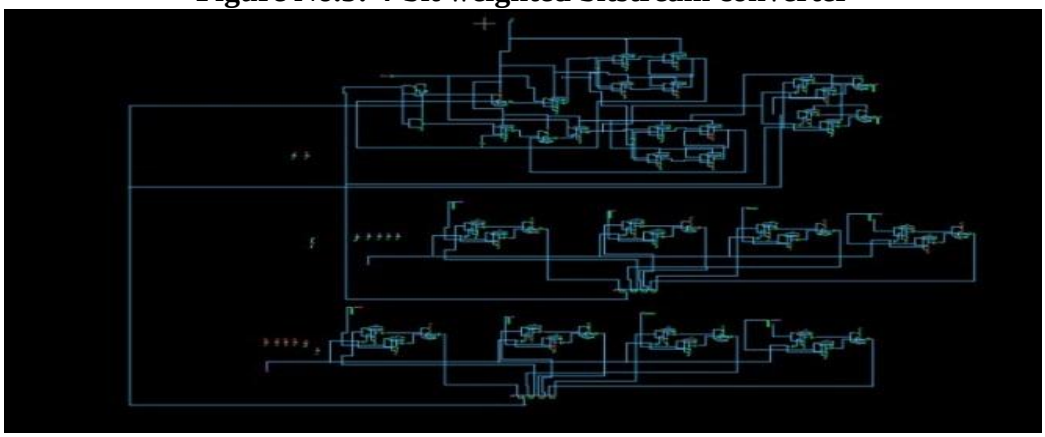

Figure No.6: Schematic of proposed Design for 4-bit

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Power Results

VV1 from time 1e-009 to 8e-008
Average power consumed -> 1.407311e-005 watts
Max power 7.939144e-004 at time 6.09674e-008
Min power 0.000000e+000 at time 8e-009


Measure information will be written to file "C:\Users\USER\AppData\Local\Temp\UPDAFOURBIT\UPDAFOURBIT.measure"

Measurement result summary
   tddelay        =   -2.085ln
```

Figure No.7: Power and delay analysis of proposed 4-bit design

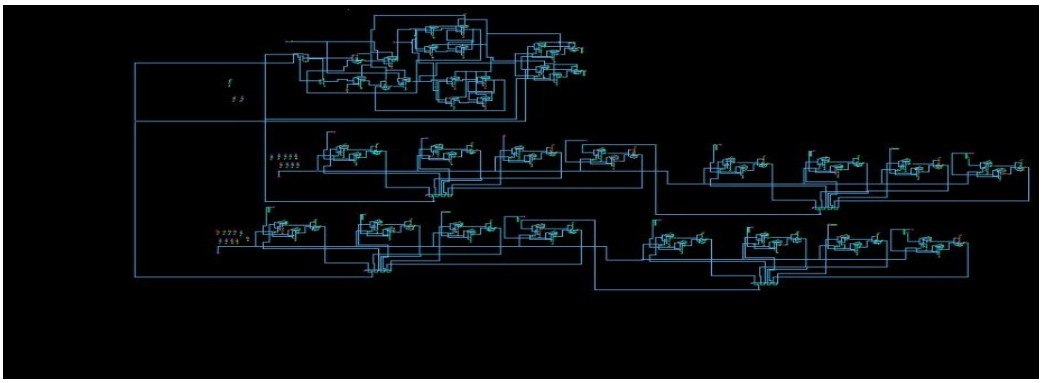

Figure No.8: Proposed Sorting network with 8-bit weighted bitstream input

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Power Results

VV1 from time 1e-009 to 2.4e-007
Average power consumed -> 1.919826e-005 watts
Max power 7.831395e-004 at time 1.80964e-007
Min power 0.000000e+000 at time 8e-009


Measure information will be written to file "C:\Users\USER\AppData\Local\Temp\EightbitLas\EightbitLas.measure"

Measurement result summary
   tddelay         =    4.3872n
```

Figure No.9: Power and Delay analysis for the proposed Sorting network with 8-bit weighted bitstream input

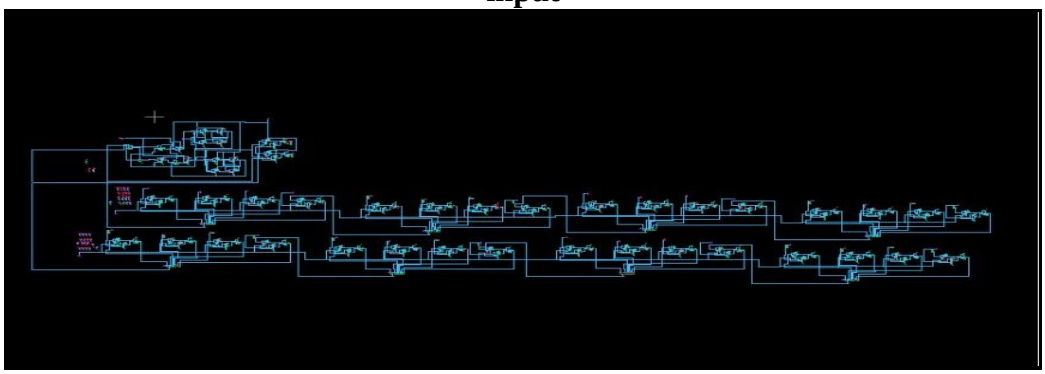

Figure No.10: Proposed sorting network with 16-bit weighted bitstream input

```
Power Results

VV1 from time 1e-009 to 2.4e-007
Average power consumed -> 5.866314e-005 watts
Max power 2.748777e-003 at time 1.80962e-007
Min power 0.000000e+000 at time 8e-009


Measure information will be written to file "C:\Users\USER\AppData\Local\Temp\sixteenbitlas\sixteenbitlas.measure"

Measurement result summary
   tddelay         =   -6.0763n


Parsing                    0.70 seconds
Setup                      1.68 seconds
```

Figure No.11: Power and Delay analysis for the proposed Sorting network with 16-bit weighted bitstream input

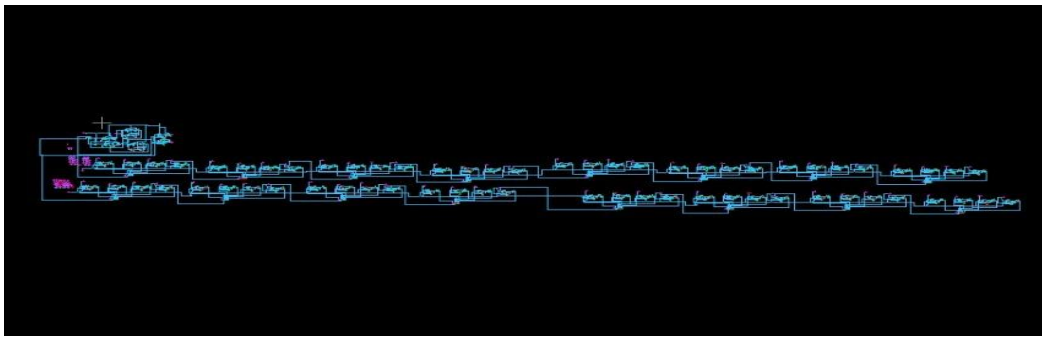

Figure No.12: Proposed Sorting network with 32-bit weighted bitstream input

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Power Results

VV1 from time 1e-009 to 6.4e-007
Average power consumed -> 1.281065e-004 watts
Max power 5.536894e-003 at time 6.09689e-008
Min power 0.000000e+000 at time 8e-009


Measure information will be written to file "C:\Users\USER\AppData\Local\Temp\thirtytwobitlas\thirtytwobitlas.measure"

Measurement result summary
   tddelay         =   -8.8890n
```

Figure No.13: Power and Delay analysis for the proposed Sorting network with 32-bit weighted bitstream input

CONCLUSION

In this work, the GDI based magnitude Comparator integrated in the sorting architecture performs superior to traditional designs in terms of power, speed and area, especially as the input bit-width increases. The architecture is proven to be scalable, efficient and well-suited for low power VLSI applications.

ACKNOWLEDGEMENT

The authors are thankful and express their sincere gratitude to Department of M.E VlSI Design, Dr. Sivanthi Aditanar College of Engineering, TamilNadu, India for providing required facilities to carry out this work.

CONFLICT OF INTEREST

We declare that we have no conflict of interest.

BIBLIOGRAPHY

1. Brady Prince, Hassan Najafi M, Bingzhe Li. Scalable low-cost sorting network with weighted bit-streams, *International Symposium on Quality Electronic Design (ISQED), IEEE-2023*, 2023, 1-6.
2. Zuodong Zhang, Runsheng Wang, Zhe Zhang, Yawen Zhang, Shaofeng Guo, Ru Huang. Circuit reliability comparison between stochastic computing and binary computing, *IEEE Transactions on Circuits and Systems II*, 67(12), 2020, 3342-3346.
3. Aditya Manjunatha, Shrinidhi Udupa, Kariyappa B S. Design of low power, area efficient 4-bit magnitude comparator using GDI logic, *Journal of Systems Engineering and Electronics*, 34(11), 2024, 1-5.
4. Mahmood Rafiee, Ebrahim Abiri. Low-power and fast-swing-restoration GDI-based magnitude comparator for digital images processing, circuits, systems and signal processing, *Springer Nature*, 41, 2022, 4848-4885.
5. Hassan Najafi M, Kia Bazargan. Low cost sorting network circuits using unary processing, *IEEE Transaction on Very Large Scale Integration*, 26(8), 2019, 1471-1480.
6. Afran Sorwar, Elias Ahammad Sojib, Md. Ashik Zafar Dipto. Design of a high-performance 2-bit magnitude comparator using hybrid logic style, *11th ICCCNT*, 2020.

7. Ebrahim Abiri, Abdolreza Darabi. Reversible logic-based magnitude comparator (RMC) circuit using modified-GDI technique for motion detection applications in image processing, *Elsevier B.V*, 72, 2019, 102928.
8. Harika D, Hari Chandana B, Nune Divya, Neelima K. Ultra-low power and high speed CNTFETs based magnitude comparator design, *12th IEEE International Conference on Communication Systems and Network Technologies*, 2023.
9. Jeevan B**,** Sivani K. Design of 64-bit signed magnitude comparator using FPGA for IOT applications, *International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI)-2022, KITS Warangal, Telangana, India*.

Please cite this article in press as: Celshiya Blessy S and Manjith R. Low power scalable sorting network using GDI-based magnitude comparator and weighted bitstream conversion, *International Journal of Engineering and Robot Technology*, 12(1), 2025, 1-9.